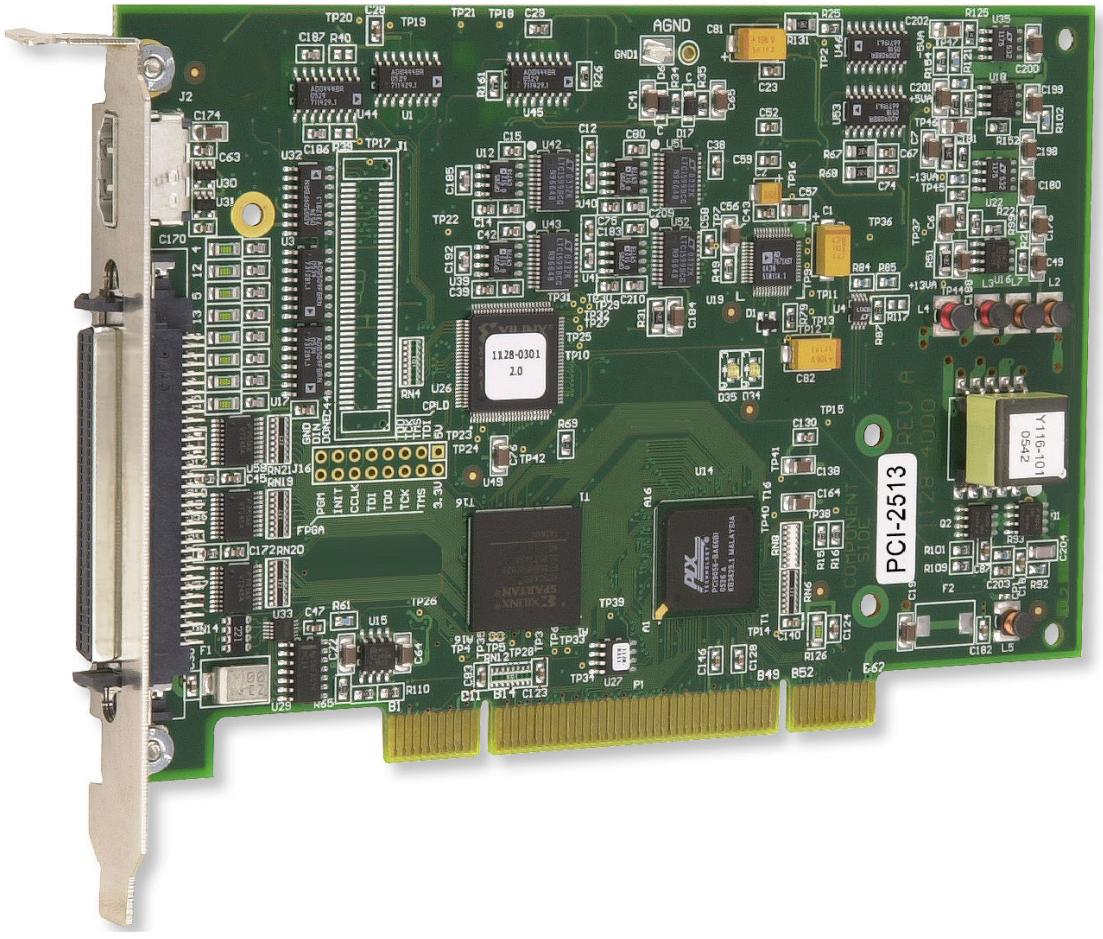
PCI-2513

16 Single-ended/8 Differential Analog Inputs

24 Digital I/O, Four 32-bit Counter Input Channels

User's Guide



MEASUREMENT COMPUTING™

PCI-2513

User's Guide

MEASUREMENT COMPUTING™

Document Revision 1, September, 2006
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About this User's Guide

What you will learn from this user's guide

This user's guide explains how to install, configure, and use the PCI-2513 so that you get the most out of its analog input, digital I/O, and counter/timer I/O features.

This user's guide also refers you to related documents available on our web site, and to technical support resources that can also help you get the most out of these boards.

Conventions used in this user's guide

For more information on …

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

<#:#> Angle brackets that enclose numbers separated by a colon signify a range of numbers, such as those assigned to registers, bit settings, etc.

bold text **Bold** text is used for the names of objects on the screen, such as buttons, text boxes, and check boxes. For example:
1. Insert the disk or CD and click the **OK** button.

italic text *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase. For example:
The *Insta*Cal installation procedure is explained in the *Quick Start Guide*.
Never touch the exposed pins or circuit connections on the board.

Where to find more information

The following electronic documents provide information that can help you get the most out of your PCI-2513.

- MCC's *Specifications: PCI-2513* (the PDF version of the *Specifications* chapter in this guide) is available on our web site at www.mccdaq.com/pdfs/PCI-2513.pdf.
- MCC's *Quick Start Guide* is available on our web site at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.
- MCC's *Guide to Signal Connections* is available on our web site at www.mccdaq.com/signals/signals.pdf.
- MCC's *Universal Library User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-user-guide.pdf.
- MCC's *Universal Library Function Reference* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-functions.pdf.
- MCC's *Universal Library for LabVIEW™ User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/SM-UL-LabVIEW.pdf.

PCI-2513 User's Guide (this document) is also available on our web site at www.mccdaq.com/PDFmanuals/PCI-2513.pdf.

Introducing the PCI-2513

Overview: PCI-2513 features

The PCI-2513 is supported under popular Microsoft® Windows® operating systems.

The PCI-2513 provides either eight differential or 16 single-ended analog inputs with 16-bit resolution. It offers seven software-selectable analog input ranges of ±10 V, ±5 V, ±2 V, ±1 V, ±0.5 V, ±0.2 V, and ±0.1V.

The board has 24 high-speed lines of digital I/O, two timer outputs, and four 32-bit counters. It provides up to 12 MHz scanning on all digital input lines.

You can operate all analog I/O, digital I/O, and counter/timer I/O synchronously and simultaneously.

Software features

For information on the features of *Insta*Cal and the other software included with your PCI-2513, refer to the *Quick Start Guide* that shipped with your device. The *Quick Start Guide* is also available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Check www.mccdaq.com/download.htm for the latest software version or versions of the software supported under less commonly used operating systems.

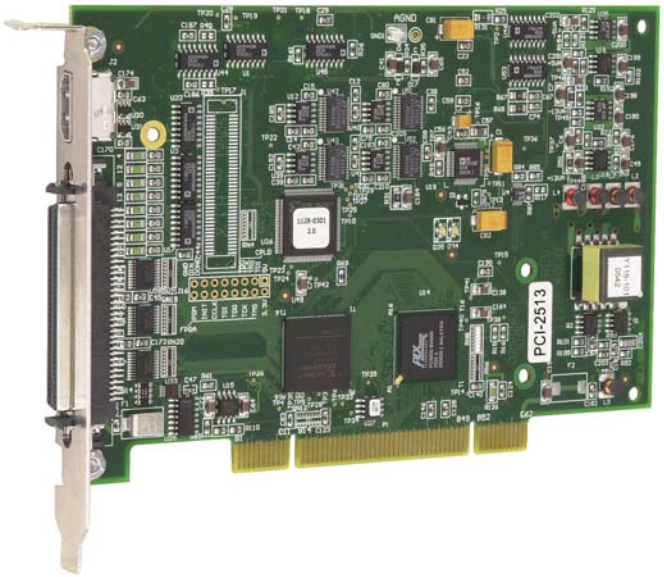
Installing the PCI-2513

What comes with your PCI-2513 shipment?

As you unpack your PCI-2513, verify that the following components are included.

Hardware

PCI-2513



Optional components

Cables and signal conditioning accessories that are compatible with the PCI-2513 are not included with PCI-2513 orders, and must be ordered separately.

If you ordered any of the following products with your board, they should be included with your shipment.

- Cables

CA-68-3R

CA-68-3S (3-feet) and CA-68-6S (6-feet)

- Signal conditioning accessories

  MCC provides signal termination products for use with the PCI-2513. Refer to the "Field wiring and signal termination" section for a complete list of compatible accessory products.

Additional documentation

In addition to this hardware user's guide, you should also receive the *Quick Start Guide* (available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf). This booklet supplies a brief description of the software you received with your PCI-2513 and information regarding installation of that software. Please read this booklet completely before installing any software or hardware.

Unpacking the PCI-2513

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the PCI-2513 from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If any components are missing or damaged, notify Measurement Computing Corporation immediately by phone, fax, or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

Installing the software

Refer to the *Quick Start Guide* for instructions on installing the software on the *Measurement Computing Data Acquisition Software CD*. This booklet is available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Installing the PCI-2513

The PCI-2513 board is completely plug-and-play. There are no switches or jumpers to set on the board. Configuration is controlled by your system's BIOS.

Before you install the PCI-2513…

Enable Bus Mastering DMA: For a PCI-2513 to operate properly, you must enable Bus Mastering DMA on the PCI slot where you will install the board. Make sure that your computer is can perform Bus Mastering DMA for the applicable PCI slot. Some computers have BIOS settings that enable and disable Bus Mastering DMA. If your computer has this BIOS option, make sure you enable Bus Mastering DMA on the appropriate PCI slot.

Refer to your PC Owner's Manual for additional information regarding your PC and enabling Bus Mastering DMA for PCI slots.

Install the MCC DAQ software: The driver needed to run your PCI-2513 is installed with the MCC DAQ software. Therefore, you need to install the MCC DAQ software before you install your board. Refer to the *Quick Start Guide* for instructions on installing the software.

To install your PCI-2513, follow the steps below.

1. Turn your computer off, open it up, and insert your board into an available PCI slot.
2. Close your computer and turn it on.

   A dialog opens as the system loads indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you are prompted for the disk containing this file. The MCC DAQ software contains this file. If required, insert the *Measurement Computing Data Acquisition Software* CD and click **OK**.

3. To test your installation and configure your board, run the *Insta*Cal utility installed in the previous section. Refer to the *Quick Start Guide* that came with your board for information on how to initially set up and load *Insta*Cal.

4. If your board has been powered-off for more than 10 minutes, allow your computer to warm up for at least 30 minutes before acquiring data. This warm-up period is required in order for the board to achieve its rated accuracy. The high speed components used on the board generate heat, and it takes this amount of time for a board to reach steady state if it has been powered off for a significant amount of time.

Allow the PCI-2513 to operate for at least 30 minutes before using the device. This warm up time is required to achieve the specified rated accuracy of measurements.

Configuring the hardware

All hardware configuration options on the PCI-2513 are software-controlled. You can select some of the configuration options using *Insta*Cal, such as the analog input configuration (16 single-ended or eight differential channels), and the edge used for pacing when using an external clock. Once selected, any program that uses the Universal Library initializes the hardware according to these selections.

Information on signal connections

General information regarding signal connection and configuration is available in the *Guide to Signal Connections*. This document is available on our web site at www.mccdaq.com/signals/signals.pdf).

Connecting the board for I/O operations

Connectors, cables – main I/O connector

Table 2-1 lists the board connectors, applicable cables, and compatible accessory products for the PCI-2513.

Table 2-1. Board connectors, cables, and compatible hardware

Connector type	68-pin standard "SCSI TYPE III" female connector HDMI connector (targeted for future expansion)
Compatible cables (for the 68-pin SCSI connector)	CA-68-3R — 68-pin ribbon cable; 3 feet. CA-68-3S — 68-pin shielded round cable; 3 feet. CA-68-6S — 68-pin shielded round cable; 6 feet.
Compatible accessory products	TB-100 terminal connector RM-TB-100

Pinout – main I/O connector

Table 2-2. PCI-2513 16-channel single-ended pin out
(8-channel differential signals in parentheses)

Signal name	Pin		Pin	Signal name
ACH0 (ACH0 HI)	68		34	ACH8 (ACH0 LO)
AGND	67		33	ACH1 (ACH1 HI)
ACH9 (ACH1 LO)	66		32	AGND
ACH2 (ACH2 HI)	65		31	ACH10 (ACH2 LO)
AGND	64		30	ACH3 (ACH3 HI)
ACH11 (ACH3 LO)	63		29	AGND
SGND	62		28	ACH4 (ACH4 HI)
ACH12 (ACH4 LO)	61		27	AGND
ACH5 (ACH5 HI)	60		26	ACH13 (ACH5 LO)
AGND	59		25	ACH6 (ACH6 HI)
ACH14 (ACH6 LO)	58		24	AGND
ACH7 (ACH7 HI)	57		23	ACH15 (ACH7 LO)
NC	56		22	N/C
NC	55		21	N/C
NEGREF	54		20	POSREF
GND	53		19	+5V
A1	52		18	A0
A3	51		17	A2
A5	50		16	A4
A7	49		15	A6
B1	48		14	B0
B3	47		13	B2
B5	46		12	B4
B7	45		11	B6
C1	44		10	C0
C3	43		9	C2
C5	42		8	C4
C7	41		7	C6
GND	40		6	TTL TRG
CNT1	39		5	CNT0
CNT3	38		4	CNT2
TMR1	37		3	TMR0
GND	36		2	XAPCR
GND	35		1	XDPCR

PCI slot ↓

Cabling

Use a CA-68-3R 68-pin ribbon expansion cable (Figure 2-1), or a CA-68-3S (3-foot) or CA-68-6S (6-foot) 68-pin shielded expansion cable (Figure 2-2) to connect signals to the PCI-2513 board.)

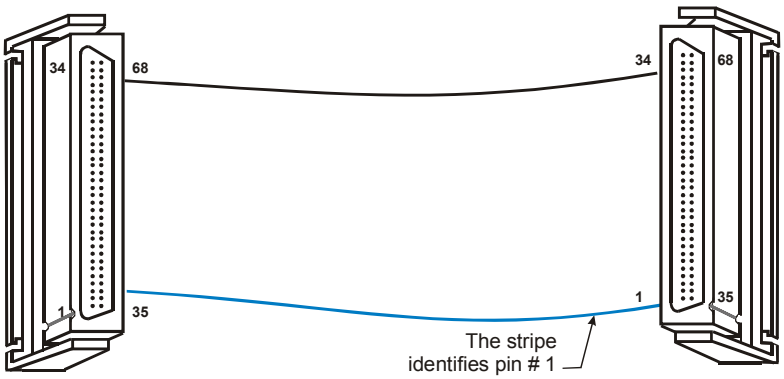


Figure 2-1. CA-68-3R cable

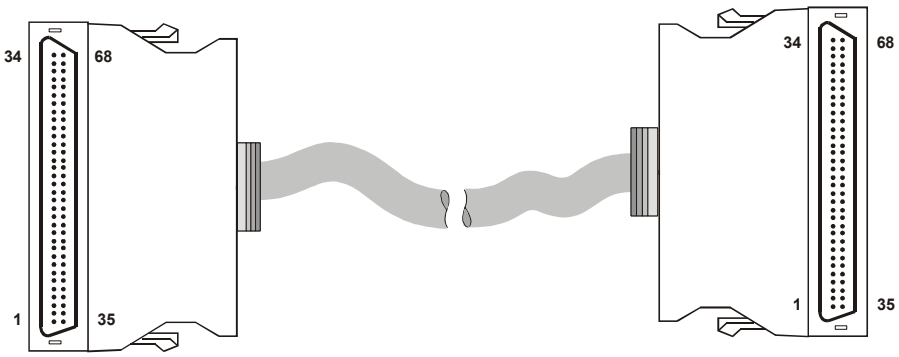


Figure 2-2. CA-68-3S and CA-68-6S cable

Field wiring and signal termination

You can use the following MCC screw terminal boards to terminate field signals and route them into the PCI-2513 board using the CA-68-3R, CA-68-3S, or CA-68-6S cable:

- **TB-100**: Termination board with screw terminals. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=98&pf_id=1787.
- **RM-TB-100**: 19-inch rack mount kit for the TB-100 termination board. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=98&pf_id=1786.

Programming and Developing Applications

After following the installation instructions in Chapter 2, your PCI-2513 should now be installed and ready for use. Although the board is part of the larger Measurement Computing hardware family, in general there may be no correspondence among registers for different boards. Software written at the register level for other models will not function correctly with your board.

Programming languages

Measurement Computing's Universal Library provides access to board functions from a variety of Windows programming languages. If you are planning to write programs, or would like to run the example programs for Visual Basic® or any other language, please refer to the *Universal Library User's Guide* (available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-user-guide.pdf).

Packaged applications programs

Many packaged application programs—such as SoftWIRE® and DASYLab™—now have drivers for your board. If the package you own does not have drivers for the board, please fax or e-mail the package name and the revision number from the install disks. We will research the package for you and advise how to obtain drivers.

Some application drivers are included with the Universal Library package, but not with the application package. If you have purchased an application package directly from the software vendor, you may need to purchase our Universal Library and drivers. Please contact us by phone, fax or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

For information on Measurement Computing applications that you can use with the PCI-2513, refer to the PCI-2513 product page at www.mccdaq.com/cbicatalog/cbiproduct_new.asp?dept_id=139&pf_id=1780.

Functional Details

This chapter contains detailed information on all of the features available from the board, including:

- a block diagram of board functions
- information on how to use, when to use, and when not to use the signals generated by the board
- diagrams of signals using default or conventional board settings

PCI-2513 block diagram

Figure 4-1 is a simplified block diagram of the PCI-2513. This board provides all of the functional elements shown in the figure.

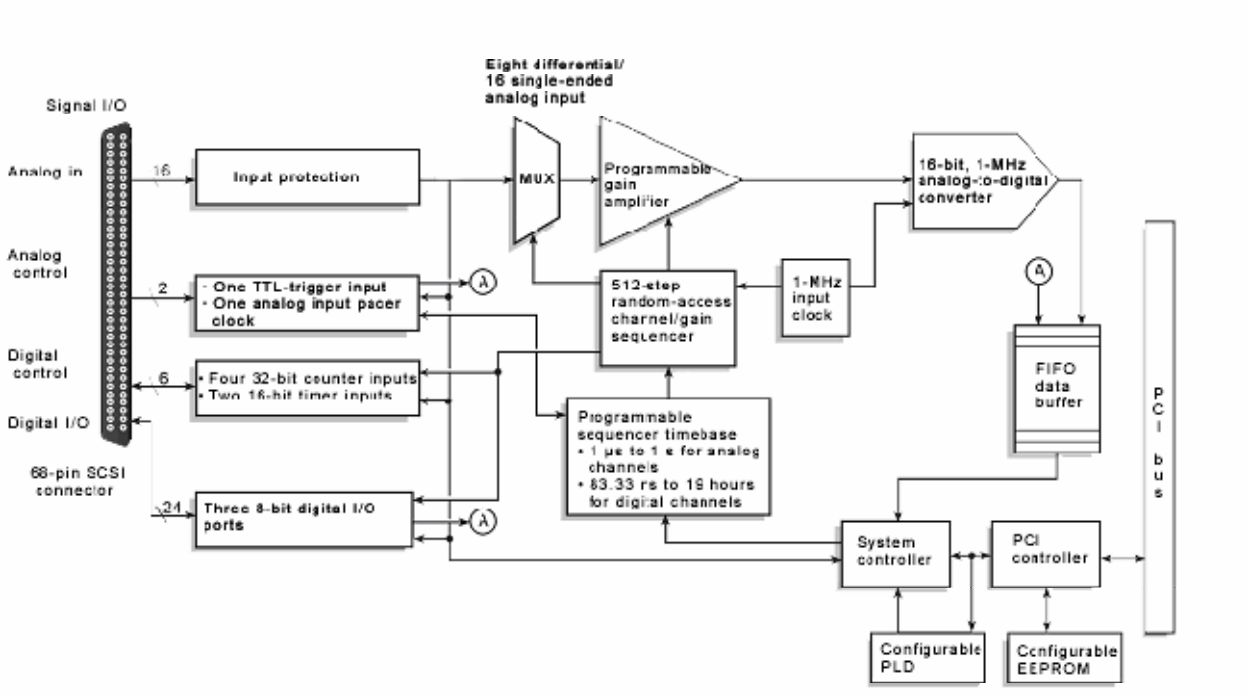


Figure 4-1. PCI-2513 functional block diagram

Synchronous I/O – mixing analog, digital, and counter scanning

The PCI-2513 can read analog, digital, and counter inputs, while generating digital pattern outputs at the same time. Digital and counter inputs do not affect the overall A/D rate because these inputs use no time slot in the scanning sequencer.

For example, one analog input channel can be scanned at the full 1 MHz A/D rate along with digital and counter input channels. Each analog channel can have a different gain, and counter and digital channels do not need additional scanning bandwidth as long as there is at least one analog channel in the scan group.

Digital input channel sampling is not done during the "dead time" of the scan period where no analog sampling is being done either.

The ability to scan digital and counter channels along with analog channels provides for a more deterministic collection of data.

Bus mastering DMA

The PCI-2513 supports bus mastering DMA. With multiple DMA channels, analog, digital, and counter input data, as well as digital output data, can flow between the PC and the PCI-2513 without consuming valuable CPU time. The driver supplied with the PCI-2513 automatically uses bus mastering DMA to efficiently conduct I/O from the PC to the PCI-2513.

Analog input

The PCI-2513 has a 16-bit, 1-MHz A/D coupled with 16 single-ended, or eight differential analog inputs. Seven software programmable ranges provide inputs from ±10 V to ±100 mV full scale.

Analog input scanning

The PCI-2513 has several scanning modes to address various applications. You can load the 512-location scan buffer with any combination of analog input channels. All analog input channels in the scan buffer are measured sequentially at 1 µs per channel.

For example, in the fastest mode, with a 0 delay between the end of scan and the start of scan, a single analog channel can be scanned continuously at 1 MS/s; two analog channels can be scanned at 500 kS/s each; 16 analog input channels can be scanned at 62.5 kS/s.

Example: Analog channel scanning of voltage inputs

Figure 4-2 shows a simple acquisition. The scan is programmed pre-acquisition and is made up of six analog channels (Ch0, Ch1, Ch3, Ch4, Ch6, Ch7). Each of these analog channels can have a different gain. The acquisition is triggered and the samples stream to the PC via DMA. Each analog channel requires one microsecond of scan time—therefore the scan period can be no shorter than 6 µs for this example. The scan period can be made much longer than 6 µs—up to 1 s. The maximum scan frequency is one divided by 6 µs or 166,666 Hz.

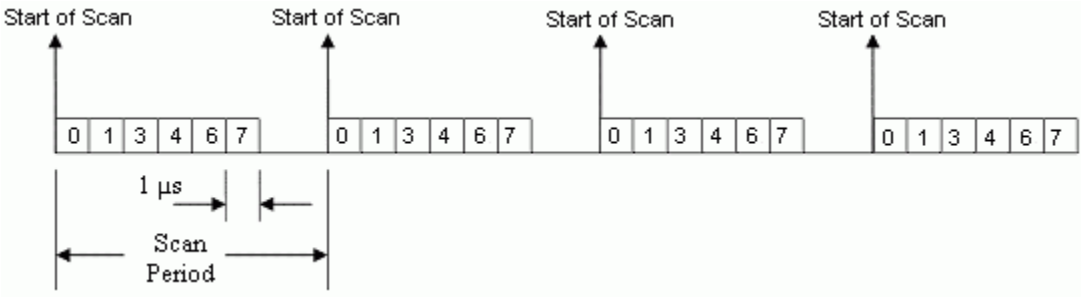


Figure 4-2. Analog channel scan of voltage inputs example

Digital I/O

Twenty-four TTL-level digital I/O lines are included in each PCI-2513. You can program digital I/O in 8-bit groups as either inputs or outputs and scan them in several modes (see "Digital input scanning" on page 17). You can access input ports asynchronously from the PC at any time, including when a scanned acquisition is occurring.

Digital input scanning

Digital input ports can be read asynchronously before, during, or after an analog input scan.

Digital input ports can be part of the scan group and *scanned along with analog input channels*. Two synchronous modes are supported when digital inputs are scanned along with analog inputs.

In both modes, adding digital input scans has no affect on the analog scan rate limitations.

If no analog inputs are being scanned, the digital inputs can be scanned at up to 12 MHz.

Digital outputs and pattern generation

Digital outputs can be updated asynchronously at anytime before, during, or after an acquisition. You can use two of the 8-bit ports to generate a digital pattern at up to 12 MHz. The PCI-2513 supports digital pattern generation with bus mastering DMA. The digital pattern can be read from PC RAM.

Digital pattern generation is clocked using an internal clock. The on-board programmable clock generates updates ranging from once every 1 second to 1 MHz, independent of any acquisition rate.

Triggering

Triggering can be the most critical aspect of a data acquisition application. The PCI-2513 supports the following trigger modes to accommodate certain measurement situations.

Hardware analog triggering

The PCI-2513 uses true analog triggering in which the trigger level you program sets an analog DAC, which is then compared in hardware to the analog input level on the selected channel. . This guarantees an analog trigger latency that is less than 1 µs.

You can select any analog channel as the trigger channel, but the selected channel must be the first channel in the scan. You can program the trigger level, the rising or falling edge, and hysteresis.

Concerning hardware analog level trigger and comparator change state

When analog input voltage starts near the trigger level, and you are performing a rising or falling] hardware analog level trigger, the analog level comparator may have already tripped before the sweep was enabled. If this is the case, the circuit waits for the comparator to change state. However, since the comparator has already changed state, the circuit does not see the transition.

To resolve this problem, do the following:

1. Set the analog level trigger to the threshold you want.
2. Apply an analog input signal that is *more than* 2.5% of the full-scale range *away from the desired threshold*. This ensures that the comparator is in the proper state at the beginning of the acquisition.
3. Bring the analog input signal toward the desired threshold. When the input signal is at the threshold (± some tolerance) the sweep will be triggered.
4. Before re-arming the trigger, again move the analog input signal to a level that is more than 2.5% of the full-scale range *away from* the desired threshold.

For example, if you are using the ±2 V full-scale range (gain = 5), and you want to trigger at +1 V on the rising edge, you would set the analog input voltage to a start value that is less than +0.9 V (1 V – (2 V * 2 * 2.5%)).

Digital triggering

A separate digital trigger input line is provided, allowing TTL-level triggering with latencies guaranteed to be less than 1 µs. You can program both of the logic levels (1 or 0) and the rising or falling edge for the discrete digital trigger input.

Software-based triggering

The three software-based trigger modes differ from hardware analog triggering and digital triggering because the readings—analog, digital, or counter—are checked by the PC in order to detect the trigger event.

Analog triggering

You can select any analog channel in the scan as the trigger channel. You can program the trigger level, the rising or falling edge, and hysteresis.

Pattern triggering

You can select any scanned digital input channel pattern to trigger an acquisition, including the ability to mask or ignore specific bits.

Counter triggering

You can program triggering to occur when one of the counters meets or exceeds a set value, or is within a range of values. You can program any of the included counter channels as the trigger source.

Software-based triggering usually results in long period of inactivity between the trigger condition being detected and the data being acquired. However, the PCI-2513 avoids this situation by using pre-trigger data. When software-based-triggering is used, and the PC detects the trigger condition—which may be thousands of readings after the actual occurrence of the signal—the PCI-2513 driver automatically looks back to the location in memory where the actual trigger-causing measurement occurred, and presents the acquired data that begins at the point where the trigger-causing measurement occurs. The maximum inactive period in this mode equals one scan period.

Set pre-trigger > 0 when using counter as trigger source

When using a counter for a trigger source, you should use a pre-trigger with a value of at least 1. Since all counters start at zero with the first scan, there is no valid reference in regard to rising or falling edge. Setting a pre-trigger to 1 or more ensures that a valid reference value is present, and that the first trigger will be legitimate.

Stop trigger modes

You can use any of the software trigger modes explained previously to stop an acquisition.

For example, you can program an acquisition to begin on one event—such as a voltage level—and then stop on another event—such as a digital pattern.

Pre-triggering and post-triggering modes

The PCI-2513 supports four modes of pre-triggering and post-triggering, providing a wide-variety of options to accommodate any measurement requirement.

When using pre-trigger, you must use software-based triggering to initiate an acquisition.

No pre-trigger, post-trigger stop event.

In this simple mode, data acquisition starts when the trigger is received, and the acquisition stops when the stop-trigger event is received.

Fixed pre-trigger with post-trigger stop event

In this mode, you set the number of pre-trigger readings to acquire. The acquisition continues until a stop-trigger event occurs.

No pre-trigger, infinite post-trigger

In this mode, no pre-trigger data is acquired. Instead, data is acquired beginning with the trigger event, and is terminated when you issue a command to halt the acquisition.

Fixed pre-trigger with infinite post-trigger

You set the amount of pre-trigger data to acquire. Then, the system continues to acquire data until the program issues a command to halt acquisition.

Counter inputs

Four 32-bit counters are built into the PCI-2513. Each counter accepts frequency inputs up to 20 MHz.

The counters can concurrently monitor time periods, frequencies, pulses, and other event driven incremental occurrences directly from pulse-generators, limit switches, proximity switches, and magnetic pick-ups.

Counter inputs can be read asynchronously under program control, or synchronously as part of an analog or digital scan group.

When reading synchronously, all counters are set to zero at the start of an acquisition. When reading asynchronously, counters may be cleared on each read, count up continually, or count until the 16 bit or 32 bit limit has been reached. See counter mode descriptions below.

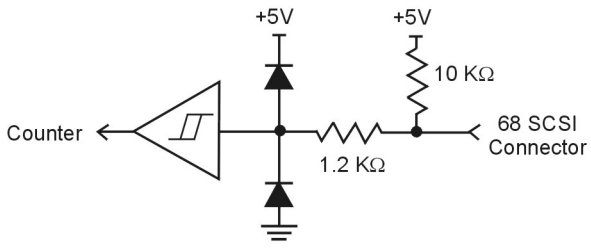


Figure 4-3. Typical PCI-2513 counter channel

Mapped channels

A *mapped channel* is one of four counter input signals that can get multiplexed into a counter module. The mapped channel can participate with the counter's input signal by gating the counter, latching the counter, and so on. The four possible choices for the mapped channel are the four counter input signals (post-debounce).

A mapped channel can be used to:

- gate the counter
- decrement the counter
- latch to current count to the count register

Usually, all counter outputs are latched at the beginning of each scan within the acquisition. However, you can use a second channel—known as the Error! Reference source not found. to latch the counter output.

Counter modes

A counter can be asynchronously read with or without *clear on read*. The asynchronous read-signals strobe when the lower 16-bits of the counter are read by software. The software can read the counter's high 16-bits some time later after reading the lower 16-bits. The full 32-bit result reflects the timing of the first asynchronous read strobe.

Totalize mode

The *Totalize modes* allows basic use of a 32-bit counter. While in this mode, the channel's input can only increment the counter upward. When used as a 16-bit counter (counter low), one channel can be scanned at the 12 MHz rate. When used as a 32-bit counter (*counter high*), two sample times are used to return the full 32-bit result. Therefore a 32-bit counter can only be sampled at a 6 MHz maximum rate. If you only want the upper 16 bits of a 32-bit counter, then you can acquire that upper word at the 12 MHz rate.

The counter counts up and does not clear on every new sample. However, it does clear at the start of a new scan command.

The counter rolls over on the 16-bit (*counter low*) boundary, or on the 32-bit (*counter high*) boundary.

Clear on read mode

The counter counts up and is cleared after each read. By default, the counter counts up and only clears the counter at the start of a new scan command. The final value of the counter —the value just before it was cleared—is latched and returned to the PCI-2513.

Stop at the top mode

The counter stops at the top of its count. The top of the count is FFFF hex (65,535) for the 16-bit mode, and FFFFFFFF hex (4,294,967,295) for the 32-bit mode.

32-bit or 16-bit

Sets the counter type to either **16-bits** or **32-bits**. The type of counter only matters if the counter is using the stop at the top mode—otherwise, this option is ignored.

Latch on map

Sets the signal on the mapped counter input to latch the count.

By default, the *start of scan* signal—a signal internal to the PCI-2513 pulses once every scan period to indicate the start of a scan group—latches the count, so the count is updated each time a scan is started.

Gating "on" mode

Sets the gating option to "on" for the mapped channel, enabling the mapped channel to gate the counter.

Any counter can be *gated* by the mapped channel. When the mapped channel is *high*, the counter is enabled. When the mapped channel is *low*, the counter is disabled (but holds the count value). The mapped channel can be any counter input channel other than the counter being gated.

Decrement "on" mode

Sets the counter decrement option to "on" for the mapped channel. The input channel for the counter increments the counter, and you can use the mapped channel to decrement the counter.

Debounce modes

Each channel's output can be debounced with 16 programmable debounce times from 500 ns to 25.5 ms. The debounce circuitry eliminates switch-induced transients typically associated with electro-mechanical devices including relays, proximity switches, and encoders.

There are two debounce modes, as well as a debounce bypass, as shown in Figure 4-4. In addition, the signal from the buffer can be inverted before it enters the debounce circuitry. The inverter is used to make the input rising-edge or falling-edge sensitive.

Edge selection is available with or without debounce. In this case the debounce time setting is ignored and the input signal goes straight from the inverter or inverter bypass to the counter module.

There are 16 different debounce times. In either debounce mode, the debounce time selected determines how fast the signal can change and still be recognized.

The two debounce modes are *trigger after stable* and *trigger before stable*. A discussion of the two modes follows.

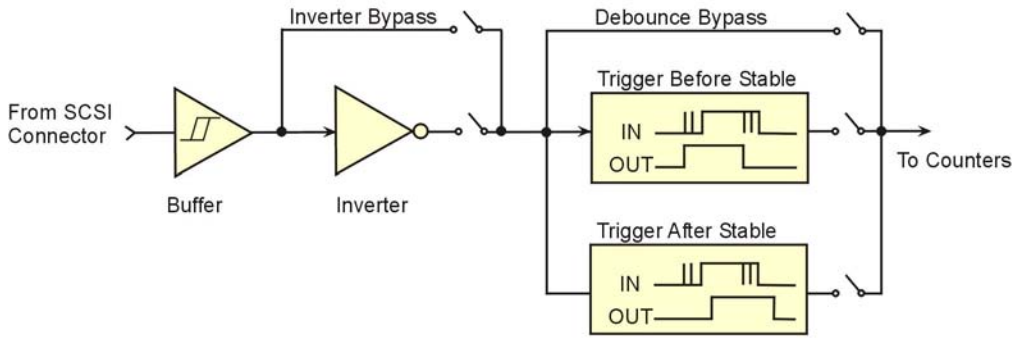


Figure 4-4. Debounce model block diagram

Trigger after stable mode

In the *trigger after stable* mode, the output of the debounce module does not change state until a period of stability has been achieved. This means that the input has an edge, and then must be stable for a period of time equal to the debounce time.

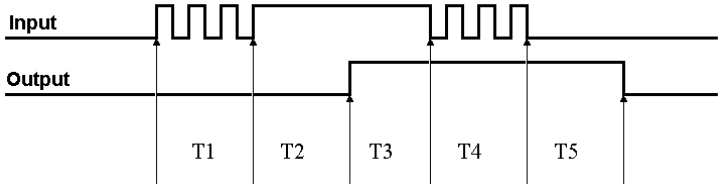


Figure 4-5. Debounce module – trigger after stable mode

The following time periods (T1 through T5) pertain to Figure 4-5. In *trigger after stable* mode, the input signal to the debounce module is required to have a period of stability after an incoming edge, in order for that edge to be accepted (passed through to the counter module.) The debounce time for this example is equal to T2 and T5.

- T1 – In the example above, the input signal goes high at the beginning of time period T1, but never stays high for a period of time equal to the debounce time setting (equal to T2 for this example.)
- T2 – At the end of time period T2, the input signal has transitioned high and stayed there for the required amount of time—therefore the output transitions high. If the input signal does not stabilize in the high state long enough, no transition would have appeared on the output and the entire disturbance on the input would have been rejected.
- T3 – During time period T3, the input signal remained steady. No change in output is seen.
- T4 – During time period T4, the input signal has more disturbances and does not stabilize in any state long enough. No change in the output is seen.
- T5 – At the end of time period T5, the input signal has transitioned low and stayed there for the required amount of time—therefore the output goes low.

Trigger before stable mode

In the *trigger before stable* mode, the output of the debounce module immediately changes state, but will not change state again until a period of stability has passed. For this reason the mode can be used to detect glitches.

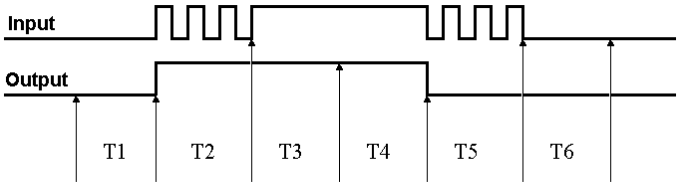


Figure 4-6. Debounce module – Trigger before stable mode

The following time periods (T1 through T6) pertain to the above drawing.

- T1 – In the illustrated example, the input signal is low for the debounce time (equal to T1); therefore when the input edge arrives at the end of time period T1, it is accepted and the output (of the debounce module) goes high. Note that a period of stability must precede the edge in order for the edge to be accepted.
- T2 – During time period T2, the input signal is not stable for a length of time equal to T1 (the debounce time setting for this example.) Therefore, the output stays "high" and does not change state during time period T2.
- T3 – During time period T3, the input signal is stable for a time period equal to T1, meeting the debounce requirement. The output is held at the high state. This is the same state as the input.
- T4 – At anytime during time period T4, the input can change state. When this happens, the output will also change state. At the end of time period T4, the input changes state, going low, and the output follows this action [by going low].
- T5 – During time period T5, the input signal again has disturbances that cause the input to not meet the debounce time requirement. The output does not change state.
- T6 – After time period T6, the input signal has been stable for the debounce time and therefore any edge on the input after time period T6 is immediately reflected in the output of the debounce module.

Debounce mode comparisons

Figure 4-7 shows how the two modes interpret the same input signal, which exhibits glitches. Notice that the *trigger before stable* mode recognizes more glitches than the *trigger after stable* mode. Use the *bypass* option to achieve maximum glitch recognition.

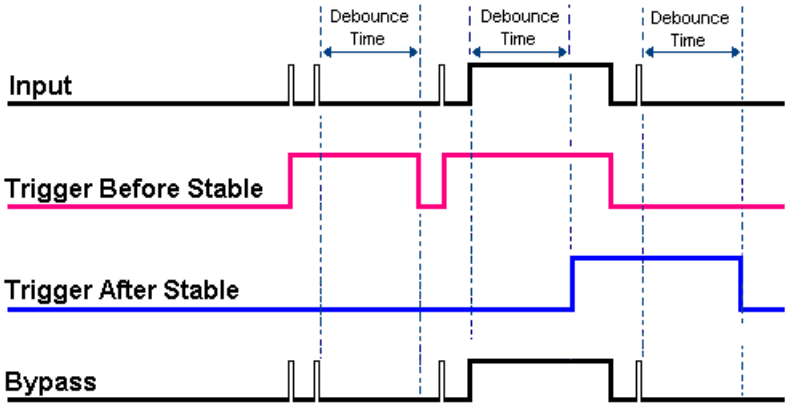


Figure 4-7. Example of two debounce modes interpreting the same signal

Debounce times should be set according to the amount of instability expected in the input signal. Setting a debounce time that is too short may result in unwanted glitches clocking the counter. Setting a debounce time too long may result in an input signal being rejected entirely. Some experimentation may be required to find the appropriate debounce time for a particular application.

To see the effects of different debounce time settings, simply view the analog waveform along with the counter output. This can be done by connecting the source to an analog input.

Use *trigger before stable* mode when the input signal has groups of glitches and each group is to be counted as one. The trigger before stable mode recognizes and counts the first glitch within a group but rejects the subsequent glitches within the group if the debounce time is set accordingly. The debounce time should be set to encompass one entire group of glitches as shown in the following diagram.

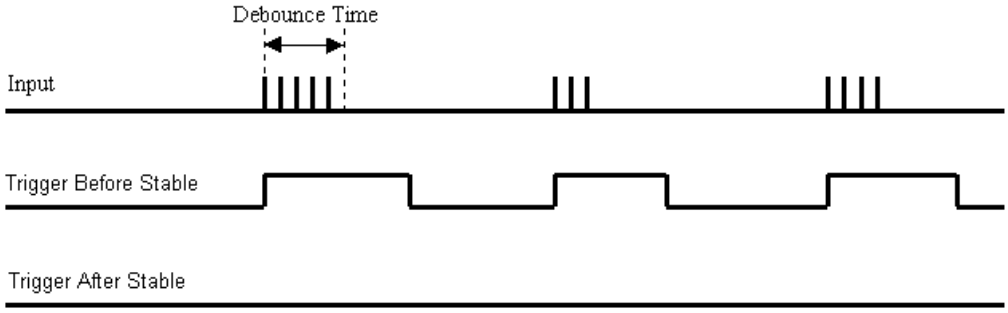


Figure 4-8.Optimal debounce time for trigger before stable mode

Trigger after stable mode behaves more like a traditional debounce function: rejecting glitches and only passing state transitions after a required period of stability. *Trigger after stable* mode is used with electro-mechanical devices like encoders and mechanical switches to reject switch bounce and disturbances due to a vibrating encoder that is not otherwise moving. The debounce time should be set short enough to accept the desired input pulse but longer than the period of the undesired disturbance as shown in Figure 4-9.

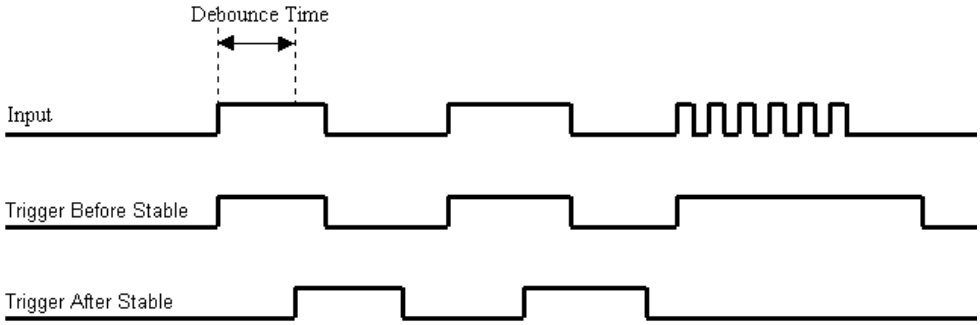


Figure 4-9. Optimal debounce time for trigger after stable mode

Timer outputs

Two 16-bit timer outputs are built into every 3000 series board. Each timer is capable of generating a different square wave with a programmable frequency in the range of 16 Hz to 1 MHz.

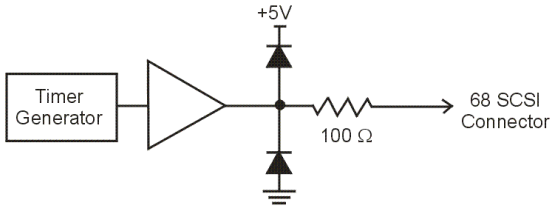


Figure 4-10. Typical PCI-2513 timer channel

Example: Timer outputs

Timer outputs are programmable square waves. The period of the square wave can be as short as 1us or as long as 65535 µs. See Table 4-3 for some examples.

Table 4-3. Timer output frequency examples

Divisor	Timer output frequency
1	1 MHz
100	10 kHz
1000	1 kHz
10000	100 Hz
65535	15.259 Hz

The two timer outputs can generate different square waves. The timer outputs can be updated asynchronously at any time.

Multiple PCI-2513s per PC

PCI-2513 features can be replicated up to four times, as up to four boards can be installed in a single host PC. The serial number on each PCI-2513 distinguishes one from another. You can operate multiple PCI-2513 boards synchronously. To do this, assign one PCI-2513 as the master.. Synchronize the other slave PCI-2513 boards to the master by the pacer clock, which is externally routed to the designated slave boards.

Calibrating the PCI-2513

Every range of a PCI-2513 device is calibrated at the factory using a digital NIST traceable calibration method. This method works by storing a correction factor for each range on the unit at the time of calibration. For analog inputs, the user can adjust the calibration of the board while it is installed in the acquisition system. This does not destroy the factory calibration supplied with the board. This is accomplished by having two distinct calibration tables in the PCI-2513 on-board EPROM—one which contains the factory calibration, and the other which is available for field calibration.

You can perform field calibration automatically in seconds with *Insta*Cal and without the use of external hardware or instruments.

Field calibration derives its traceability through an on-board reference which has a stability of 0.005% per year.

Note that a two-year calibration period is recommended for PCI-2513 boards.

You should calibrate the PCI-2513 using *Insta*Cal after the board has fully warmed up. The recommended warm-up time is 30 minutes. For best results, calibrate the board immediately before making critical measurements. The high resolution analog components on the board are somewhat sensitive to temperature. Pre-measurement calibration ensures that your board is operating at optimum calibration values.

Specifications

Typical for 25 °C unless otherwise specified.
Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	Successive approximation
Resolution	16 bits
Number of channels	16 single-ended/8 differential, software-selectable
Input ranges (SW programmable)	Bipolar: ±10 V, ±5 V, ±2 V, ±1 V , ±0.5 V, ±0.2 V, ±0.1 V
Maximum sample rate	1 MHz
Nonlinearity (integral)	±2 LSB maximum
Nonlinearity (differential)	±1 LSB maximum
A/D pacing	On board A/D clock, external source (XAPCR)
Trigger sources and modes	See Table 6
Data transfer	DMA
Configuration memory	Programmable I/O
Maximum usable input voltage + common mode voltage (CMV + V_{in})	Range: ±10 V, ±5 V, ±2 V, ±1 V , ±0.5 V 10.5 V maximum Range: ±0.2 V, ±0.1 V 2.1 V maximum
Signal to noise and distortion	*72 dB typical for ±10 V range, 1 kHz fundamental*
Total harmonic distortion	*-80 dB typical for ±10 V range, 1 kHz fundamental*
Calibration	Auto-calibration, calibration factors for each range stored on the board in non-volatile RAM.
CMRR @ 60 Hz	-70 dB typical DC to 1 kHz
Bias current	*40 pA typical (0 °C to 35°C)*
Input impedance	*10 MΩ single-ended, 20 MΩ differential*
Absolute maximum input voltage	*±30 V*

Accuracy

Table 2. Analog input accuracy specifications

Voltage range		**Accuracy ±(% of reading + % range) 23°C ±10 °C, 1 year**	**Temperature coefficient ±(ppm of reading + ppm range)/°C**	***Noise (cts RMS)***	
-10 V to 10 V	Note 1	0.031% + 0.008%	14 + 8	*1.5*	*Note 2*
-5 V to 5 V		0.031% + 0.009%	14 + 9	*2.0*	
-2 V to 2 V		0.031% + 0.010%	14 +10	*1.6*	
-1 V to 1 V		0.031% + 0.02%	14 + 12	*2.5*	
-500 mV to 500 mV		0.031% + 0.04%	14 +18	*4.0*	
-200 mV to 200 mV		0.036% + 0.075%	14 +12	*5.0*	
-100 mV to 100 mV		0.042% + 0.15%	14 +18	*9.0*	

Note 1: Specifications assume differential input single-channel scan, 1 MHz scan rate, unfiltered, CMV=0.0 V, 30 minute warm-up, exclusive of noise.

Note 2: Noise reflects 10,000 samples at 1 MHz, typical, differential short, using CA-68-3S cable.

Digital input / output

Table 3. Digital input/output specifications

Number of I/O	24
Ports	Three banks of 8. Each port is programmable as input or output
Input scanning mode	Asynchronous, under program control at any time relative to input scanning
Configuration	10 kΩ pull-up to +5 V, 20 pf to analog common
Input protection	±15 kV ESD clamp diodes
Input high	*+2.0 V to +5.0 V*
Input low	*0 to 0.8 V*
Output high	*>2.0 V*
Output low	*<0.8 V*
Output current	Output 12 mA per pin, 200 mA total continuous
Digital input pacing	Onboard clock, external clock (XAPCR)
Digital output pacing	Four programmable sources: ▪ Onboard D/A clock, independent of scanning input clock ▪ Onboard scanning input clock ▪ External D/A input clock, independent of external scanning input clock-(XDPCR) ▪ External scanning input clock-(XAPCR)
Digital input trigger sources and modes	See Table 6
Digital output trigger sources	Start of input scan
Data transfer	DMA
Sampling/update rate	12 MHz maximum
Pattern generation output	Two of the 8-bit ports can be configured for 16-bit pattern generation. The pattern can also be updated synchronously with an acquisition at up to 12 MHz.

Counters

Counter inputs can be scanned based on an internal programmable timer or an external clock source.

Table 4. Counter specifications

Channels	Four independent
Resolution	32-bit
Input frequency	20 MHz maximum
Input signal range	-5 V to 10 V
Input characteristics	10 kΩ pull-up, ±15 kV ESD protection
Trigger level	TTL
Minimum pulse width	25 ns high, 25 ns low
De-bounce times	16 selections from 500 ns to 25.5 ms, positive or negative edge sensitive, glitch detect mode or de-bounce mode
Time-base accuracy	30 ppm (0 ° to 50 °C)
Counter read pacer	On board clock, external clock (XAPCR)
Trigger sources and modes	See Table 6
Programmable mode	Counter
Counter mode options	Totalize, clear on read, rollover, stop at all Fs, 16- or 32-bit, any other channel can gate the counter

Input sequencer

Analog, digital, and counter inputs can be scanned based on either an internal programmable timer or an external clock source.

Table 5. Input sequencer specifications

Scan clock sources: two (Note 3**Error! Reference source not found.**)	Internal: ▪ Analog channels from 1 µs to 1 sec in 20.83 ns steps. ▪ Digital channels and counters from 83.33 ns to 1 sec in 20.83 ns steps. External. TTL-level input: ▪ Analog channels down to 1 µs minimum ▪ Digital channels and counters down to 83 ns minimum
Programmable parameters per scan	▪ Programmable channels (random order) ▪ Programmable gain
Depth	512 locations
Onboard channel-to-channel scan rate	Analog: 1 MHz maximum Digital: 12 MHz
External acquisition scan clock input maximum rate	1.0 MHz
Clock signal range:	Logical zero: 0 V to 0.8 V Logical one: 2.4 V to 5.0 V
Minimum pulse width	50 ns high, 50 ns low

Note 3: The maximum scan clock rate is the inverse of the minimum scan period. The minimum scan period is equal to 1 µs times the number of analog channels. If a scan contains only digital channels then the minimum scan period is 83 ns times the number of digital channels.

Trigger sources and modes

Table 6. Trigger sources and modes

Input scan trigger sources	▪ Single channel analog hardware trigger ▪ Single channel analog software trigger ▪ External-single channel digital trigger (TTL TRG input) ▪ Digital pattern trigger ▪ Counter/totalizer trigger
Input scan triggering modes	Single channel analog hardware trigger: The first analog input channel in the scan is the analog trigger channel. ▪ Input signal range: -10 V to +10 V maximum ▪ Trigger level: Programmable (12-bit resolution) ▪ Latency: 350 ns typical ▪ Accuracy: ±0.5% of reading, ±2 mV offset maximum ▪ Noise: 2 mV RMS typical
	Single channel analog software trigger: The first analog input channel in the scan is the analog trigger channel. ▪ Input signal range: Anywhere within range of the trigger channel ▪ Trigger level: Programmable (16-bit resolution) ▪ Latency: One scan period (maximum)
	External-single channel digital trigger (TTL trigger input): ▪ Input signal range: -15 V to +15 V maximum ▪ Trigger level: TTL-level sensitive ▪ Minimum pulse width: 50 ns high, 50 ns low ▪ Latency: One scan period maximum
	Digital pattern triggering: 8-bit or 16-bit pattern triggering on any of the digital ports. Programmable for trigger on equal, not equal, above, or below a value. Individual bits can be masked for "don't care" condition. Latency: One scan period, max
	Counter/totalizer triggering: Counter/totalizer inputs can trigger an acquisition. User can select to trigger on a frequency or on total counts that are equal, not equal, above, or below a value, or within/outside of a window rising/falling edge. Latency: One scan period, maximum

Frequency/pulse generators

Table 7. Frequency/pulse generator specifications

Channels	2 x 16-bit
Output waveform	Square wave
Output rate	1 MHz base rate divided by 1 to 65535 (programmable)
High-level output voltage	2.0 V minimum @ -1.0 mA, 2.9 V minimum @ -400 µA
Low-level output voltage	0.4 V maximum @ 400 µA

Power consumption

Table 8. Power consumption specifications

Power consumption (per board)	3 W

PCI compatibility

Table 9. PCI compatibility specifications

PCI bus	PCI r2.2 compliant, universal 3.3 V/5 V signaling support, compatible with PCI-X

Environmental

Table 10. Environmental specifications

Operating temperature range	0 °C to +60 °C
Storage temperature range	-40 °C to +80 °C
Relative humidity	0 to 95% non-condensing

Mechanical

Table 11. Mechanical specifications

Vibration	MIL STD 810E cat 1 and 10
Dimensions	165 mm (W) x 15 mm (D) x 108 mm (H) (6.5” x 0.6” x 4.2”)
Weight	160 g (0.35 lbs)

Main connector and pin out

Table 12. Main connector specifications

Connector type	68-pin standard "SCSI TYPE III" female connector HDMI connector (targeted for future expansion)
Compatible cables (for the 68-pin SCSI connector)	CA-68-3R — 68-pin ribbon cable; 3 feet. CA-68-3S — 68-pin shielded round cable; 3 feet. CA-68-6S — 68-pin shielded round cable; 6 feet.
Compatible accessory products	TB-100 termination board with screw terminals
	RM-TB-100, 19-inch rack mount kit for TB-100

Table 13. 16-channel single-ended pin out

Pin	Function	Pin	Function
68	ACH0	34	ACH8
67	AGND	33	ACH1
66	ACH9	32	AGND
65	ACH2	31	ACH10
64	AGND	30	ACH3
63	ACH11	29	AGND
62	SGND	28	ACH4
61	ACH12	27	AGND
60	ACH5	26	ACH13
59	AGND	25	ACH6
58	ACH14	24	AGND
57	ACH7	23	ACH15
56	NC	22	NC
55	NC	21	NC
54	NEGREF	20	POSREF
53	GND	19	+5V
52	A1	18	A0
51	A3	17	A2
50	A5	16	A4
49	A7	15	A6
48	B1	14	B0
47	B3	13	B2
46	B5	12	B4
45	B7	11	B6
44	C1	10	C0
43	C3	9	C2
42	C5	8	C4
41	C7	7	C6
40	GND	6	TTL TRG
39	CNT1	5	CNT0
38	CNT3	4	CNT2
37	TMR1	3	TMR0
36	GND	2	XAPCR
35	GND	1	XDPCR

Table 14. 8-channel differential pin out

Pin	Function	Pin	Function
68	ACH0 HI	34	ACH0 LO
67	AGND	33	ACH1 HI
66	ACH1 LO	32	AGND
65	ACH2 HI	31	ACH2 LO
64	AGND	30	ACH3 HI
63	ACH3 LO	29	AGND
62	SGND	28	ACH4 HI
61	ACH4 LO	27	AGND
60	ACH5 HI	26	ACH5 LO
59	AGND	25	ACH6 HI
58	ACH6 LO	24	AGND
57	ACH7 HI	23	ACH7 LO
56	NC	22	NC
55	NC	21	NC
54	NEGREF	20	POSREF
53	GND	19	+5V
52	A1	18	A0
51	A3	17	A2
50	A5	16	A4
49	A7	15	A6
48	B1	14	B0
47	B3	13	B2
46	B5	12	B4
45	B7	11	B6
44	C1	10	C0
43	C3	9	C2
42	C5	8	C4
41	C7	7	C6
40	GND	6	TTL TRG
39	CNT1	5	CNT0
38	CNT3	4	CNT2
37	TMR1	3	TMR0
36	GND	2	XAPCR
35	GND	1	XDPCR

CE Declaration of Conformity

Manufacturer:	IOTech, Incorporated
Address:	25971 Cannon Road Cleveland, OH 44146 USA
Category:	Information technology equipment.

IOTech, Incorporated declares under sole responsibility that the product

PCI-2513

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EU EMC Directive 89/336/EEC: Electromagnetic Compatibility, EN 61326 (1997) Amendment 1 (1998)

Emissions: Group 1, Class A

- EN 55022 (1990)/CISPR 22: Radiated and Conducted emissions.

Immunity: EN61326, Annex A

- IEC 61000-4-2 (1995): Electrostatic Discharge immunity, Criteria B.
- IEC 61000-4-3 (1995): Radiated Electromagnetic Field immunity Criteria A.
- IEC 61000-4-4 (1995): Electric Fast Transient Burst immunity Criteria B.
- IEC 61000-4-5 (1995): Surge immunity Criteria A.
- IEC 61000-4-6 (1996): Radio Frequency Common Mode immunity Criteria A.

To maintain the safety, emission, and immunity standards of this declaration, the following conditions must be met.

- Part CA-68-3S or CA-68-6S must be properly installed.
- The host computer, peripheral equipment, power sources, and expansion hardware must be CE compliant.
- All I/O cables must be shielded, with the shields connected to CHASSIS ground stud.
- I/O cables must be less than 3 meters (9.75 feet) in length.
- The host computer must be properly grounded.
- Equipment must be operated in a controlled electromagnetic environment as defined by Standards EN 61326:1998, or IEC 61326:1998.

Note: Data acquisition equipment may exhibit noise or increased offsets when exposed to high RF fields (>3V/m) or transients.

Declaration of Conformity based on tests conducted by Smith Electronics, Inc., Cleveland, OH 44141, USA in December, 2005. Test records are outlined in Smith Electronics Test Report “Daqboard 3000 with PDQ30 Expansion Module”.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

Paul Wittibschlager

Director of Hardware Engineering

Measurement Computing Corporation
10 Commerce Way
Suite 1008
Norton, Massachusetts 02766
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@mccdaq.com
www.mccdaq.com